

In the Drawings:

Fig. 1 has been amended to remove duplicate label "28" from the cathode of diode 29. Contact 28 remains. Word line 19 has been redrawn and word line 119 has been added for consistency with Figs. 2 & 4.

Fig. 4 has been amended to re-designate unidentified line "201" to "103." Line '33" has been relabeled "36" for consistency with Figs. 1 & 2.

Fig. 8 has been amended to re-designate element (Nwell) "119" as element "140." Word line 119 is present in Figs. 2 & 3.

Amended drawings and the marked-up preceding versions are attached.

Remarks

Objections to the Drawings

The Examiner suggested several minor changes to the drawings to correct discrepancies. Each suggestion is discussed in turn.

Element 28 of Fig. 1: The designation of the anode of diode 29 as element "28" has been removed. Element "28" remains a contact of transistor 23.

Device 25 of Figs. 1, 2, and 4: Applicant assumes that where the Examiner states "Fig. 2 shows a connection between transistor 25 and contact point 32; whereas Fig. 3 shows no such connection relation between these two components," the Examiner intended to indicate Figs. 1 and 2, vice Figs. 2 and 3, respectively, as device 25 is shown in Figs. 1 & 2, but not Fig. 3. Both drawings are as intended. Fig. 1 merely illustrates a relationship between word line 19, device 25, and transistor 23. The reference to "transistor 25" has been removed from the specification; references to device 25 remain. Device 25 is identified as a capacitive device in the specification.

Fig. 2 provides a clearer representation of the relationship between word line 19 and transistor 23. Word line 19 lies over capacitive plate 30, forming capacitive device 25. Tang 86' of capacitive device 25 forms a gate of transistor 23. Contact 32 is connected to the drain of transistor 23.

Line 201 of Fig. 4: Element 201 has been re-designated "actuation line 103". Element number 101 is present in Fig. 3. Element 201 is present in Fig. 8. The reference in the specification to "shared line 101" has been deleted.

Nwell 119 of Fig. 8: Fig. 8 has been revised. Element 119 has been re-designated "103;" the label "10+" has been changed to "P+" to correct a scrivener's error.

The specification has been amended to reflect all changes to the drawings.

Arguments

In the Office action mailed December 27, 2005, claims 1-12 and claim 20 were allowed. (Office action, pages 5-8.) Applicant thanks the Examiner for guidance to patentable subject matter.

Rejection of claim 21 under 35 U.S.C. §102

In order to anticipate a claim, a reference must teach all the elements of a claim. See Verdegaal Bros., Inc. v. Union Oil Co., 814 F.2d 628, 631 (Fed. Cir. 1987). In addition, the reference must show the claimed invention "in as complete detail as is contained in the patent claim" in order to anticipate the claimed invention. Richardson v. Suzuki Motor Co., Ltd., 868 F.2d 1226, 1236 (Fed. Cir. 1989). Applicant contends that the cited reference does not teach all the elements of Applicant's claim 21 and therefore claim 21 is not anticipated.

Claim 21

On page 5 of the above indicated Office action, the Examiner rejected Applicant's claim 21 as being anticipated by U.S. Pat. App. Pub. No. 2002/0014642 to Gerber et al. ("Gerber"). Applicant respectfully traverses.

Applicant asserts that Applicant's claim 21 is patentably distinguishable from the cited art as Gerber does not teach "writing data to the selected memory cell; and, simultaneously using said word line to select a second memory cell and erasing data whereby a single word line selects two memory cells for simultaneous write and erase operations" as required by Applicant's amended claim 21. The Examiner cites Gerber's paragraph 0036, which merely recites "independently programmable memory units" which "may be simultaneously

addressed by the write and erase memory operations." Gerber, [0036].

The Examiner also refers to Fig. 5 in support of his conclusion that Gerber reads on Applicant's claim 21. Gerber's specification reads: "FIG. 5 is a schematic diagram of the present invention for a write operation." Gerber [0026]. While paragraph 0040 recites that the memory segments may be independently erased or programmed, the specification and drawings do not teach or suggest that the memory segments may be programmed and erased simultaneously.

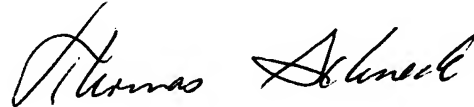
Gerber specifically provides for separate write and erase operation. "FIG. 5 is a schematic diagram of the present invention for a write operation." Gerber [0026]. "FIG. 6 is a schematic diagram of the present invention for an erase operation." Gerber [0027]. In the detailed description, paragraph 0046 recites a write operation; paragraph 0047 recites an independent erase operation. The two operations are clearly distinct and do not occur simultaneously. The cited patent's only occurrence of the word "simultaneously" appears in paragraph 0036, quoted above. No suggestion is made anywhere in the patent that write and erase operations occur at the same time.

As Gerber does not teach "simultaneous write and erase operations," as set forth in claim 21, lines 10 and 11, the cited art does not anticipate Applicant's claim 21; therefore, Applicant requests that the 35 U.S.C. § 102(b) rejection of claim 21 be withdrawn.

Conclusion

Applicant requests that the Examiner withdraw the rejection of Applicant's claim 21 in light of the arguments presented above. Applicant asserts that the application as amended is in a condition for allowance. A Notice of Allowance is earnestly solicited.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Typed Name: Merle P. Garcia
Date: March 15, 2006

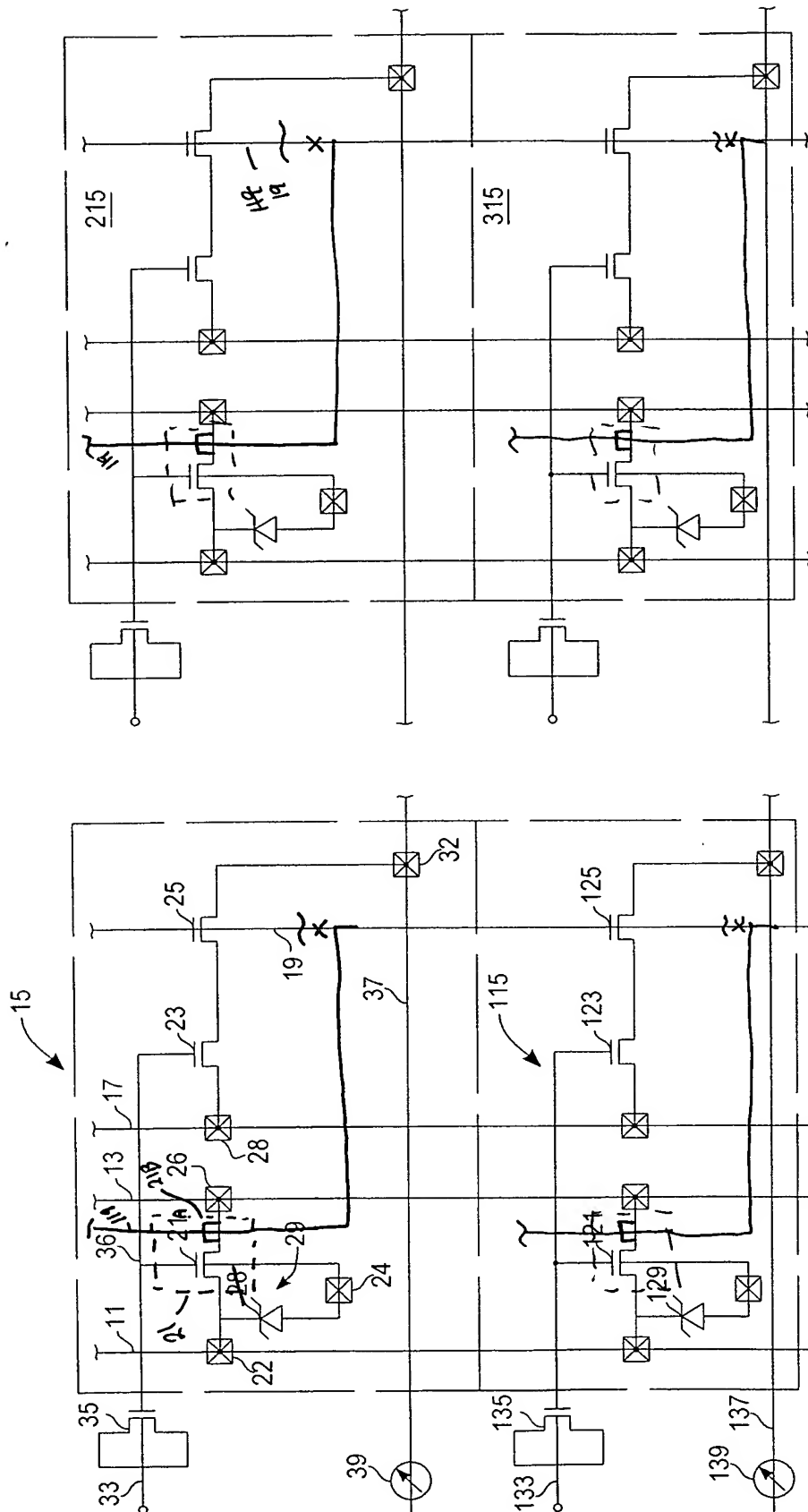


Fig. 1

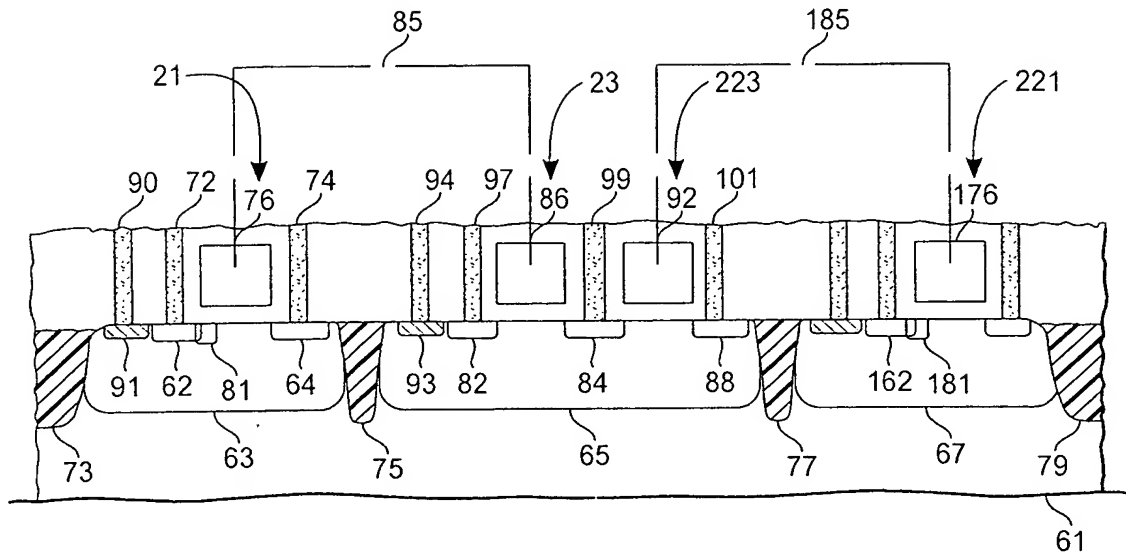


Fig. 3

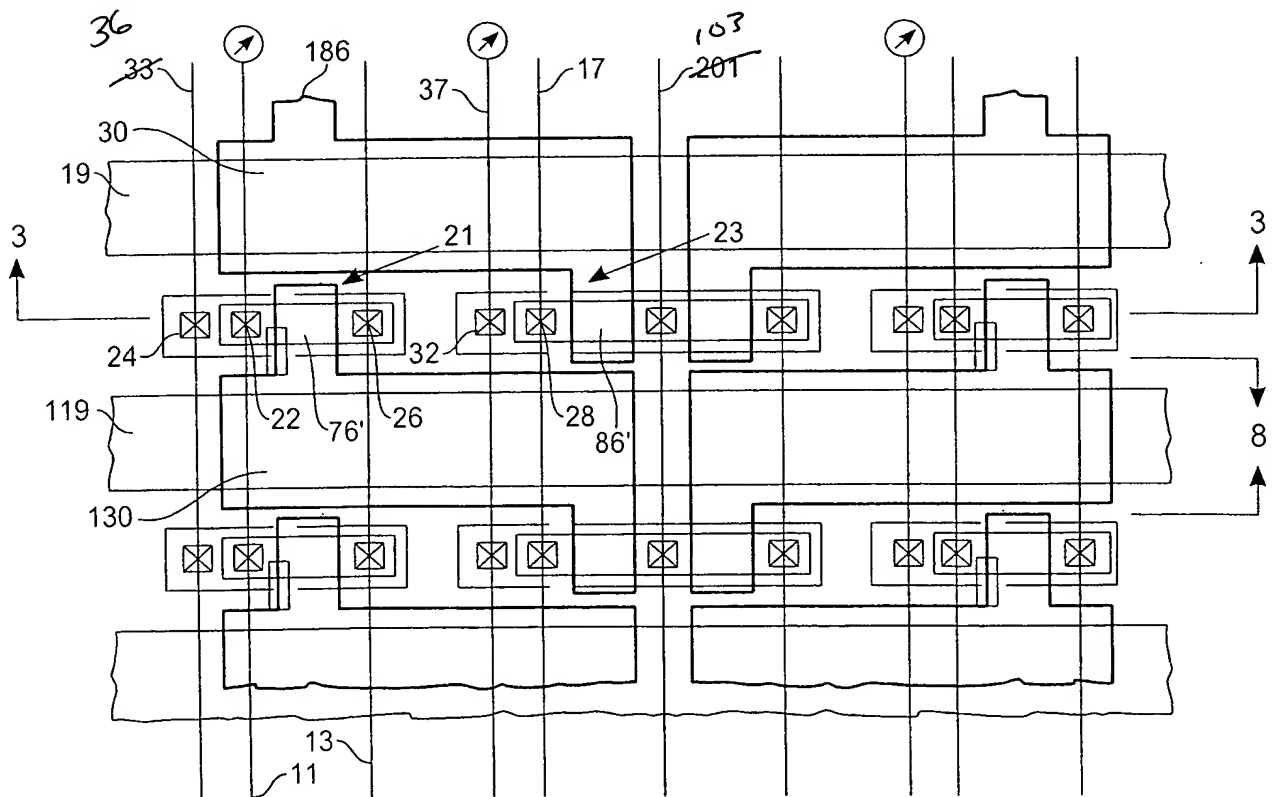


Fig. 4

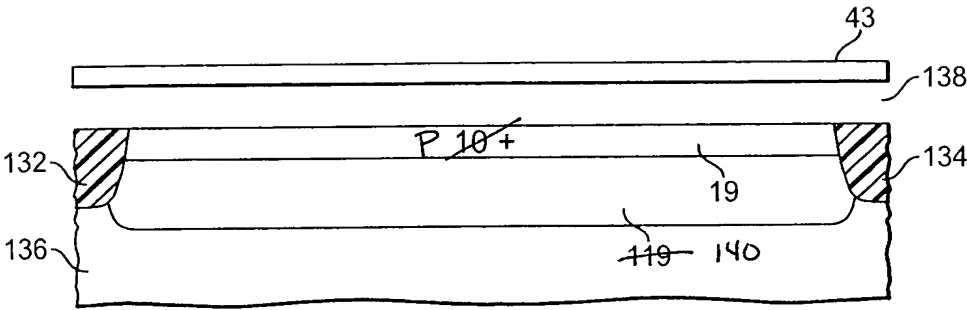


Fig. 8